Barry's System 12228 Interface

By

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Introduction

I would like to propose an Interface for the Mother board and or architecture that I designed based on 12228 bits. This was originally published back in 2013 and has been enhanced and improved and reflects updated Cyber Security issues that have been needed and required. I believe that one size does not fit all and with that being said the audience I am trying to design this for is Low End Servers with less than 100 employees. The features of this Design will provide the following:

1). 12228 bits Interface coupled with my copyrighted Model Super Sonic 12 Motherboard- Design and 12288 Bit Architecture-2011 for Low End Servers.

2). Backward compatibility to 8192 bits.

3). Linear and Curvature MAC Address specifications

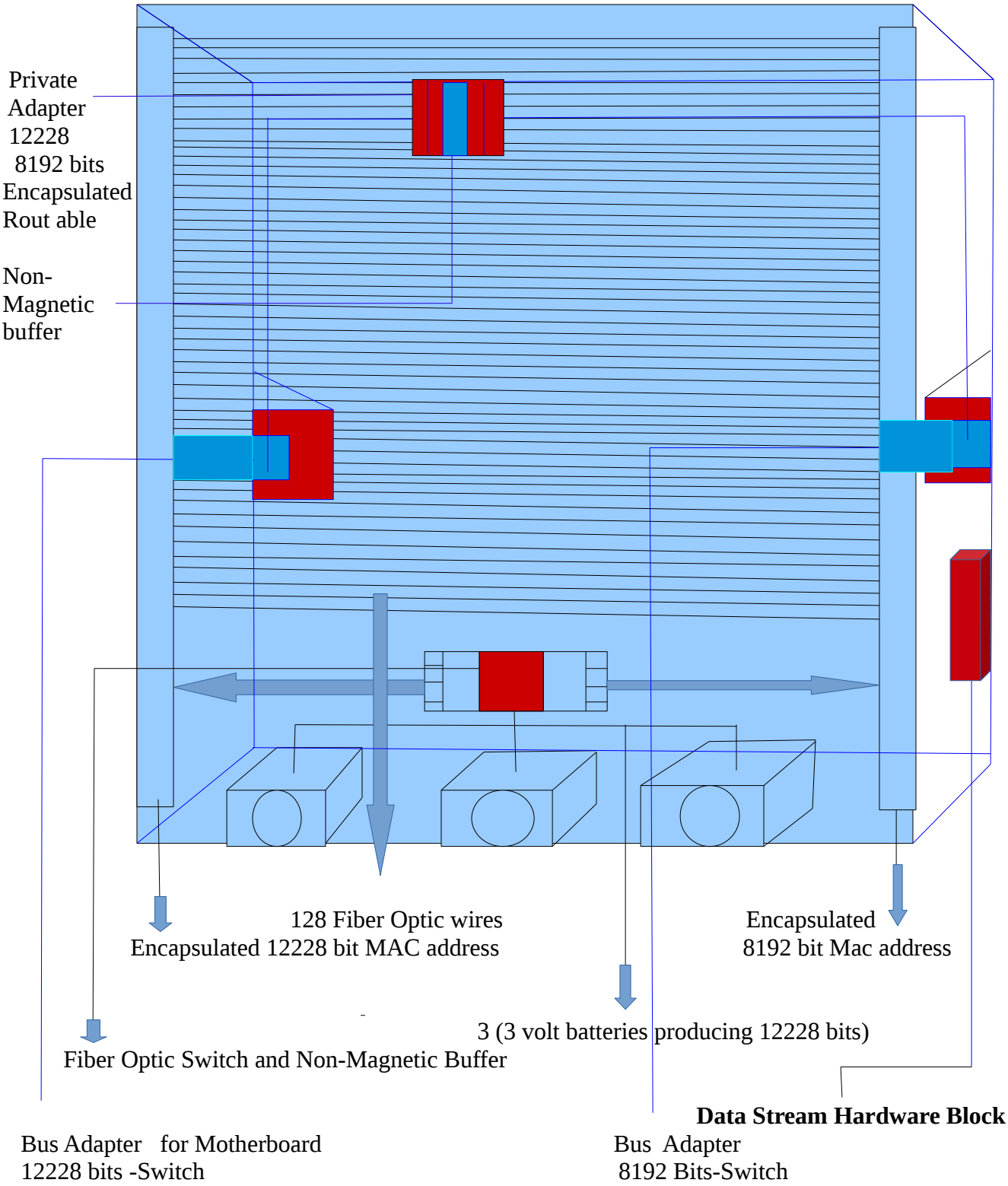
I would like to take the time to say “Thank you” for reading this Design concept.

Contents

Chapter 1

System Design

Interface Design 1-A Front View



Features of the 12228 System Interface

I would now like to go over the 12228 System Interface that is used in my Motherboard Design copyrighted Model Super Sonic 12 Motherboard- Design and 12288 Bit Architecture-2011 .

The System Interface and Motherboard have 2 separate boards for better heat tolerance and avoiding system bottlenecks because the Interface uses 128 wires with 2 bits per wire. The 12228 System Interface is backward compatible to the 8192 bit system with compression and padding to allow up to 4 combination's see chart below.

8192	**Padding**	**Compression**	**Event**
	no	No	1
	yes	no	2
12228	no	no	3
	no	yes	4

As you can see, I create 4 events including padding and compression, The diagram shows that 3 (3) volt batteries are utilized to create the 12228 system interface. This I feel should be separate from the regular BIOS settings but has interface capabilities thus creating a Dynamic Environment that is Non-Static. The linear MAC addresses utilize the following below :

Linear motion Mac Address

Bit strength	**Characters per field**	**Total**
12228	8	64
8192	4	32

The 12228 System Interface pushes 256 bits per wire at a rate of 128 wires 2 bits per wire for a total of 256 utilizing Fiber optic wire that is encased in glass tube that can tolerate heat up to 2300 degrees Fahrenheit.

The Non-Routable switch on the 12228 System Interface offers a choice between 8192 and 12228 bits that is encapsulated and sent to the Motherboard where the same method is used to protect the Mac-Address and than it is sent to the Private Adapter and binded to a private reserve IP address examples 192.168.x.x , 10.x.x.x as examples. The tunnel is created to allow for secure communications to proceed hint -Public Address space. I would recommend a new set of Authentication protocols to be developed that will insure data delivery and Integrity.

The Private Adapters-Motherboard and Interface Switch has a Non-Magnetic buffer to prevent Electromagnetic Cross talk in other words bits basically becoming entangled with one another during switch operations (OSI Bytes to Frames Non-Routable protocol 2nd layer). I would now like to present the Specifications in the next chapter. I would also like to recommend before going on to the next chapter Please take time to review the 7 layer OSI stack protocol understanding the differences between switches Non-Rout able 2nd layer and 3rd layer IP Routers Routable as a example. Please see Chart below:

Hardware	**Rout able**	**Board**
Switch	no	System 12228 Interface
Switch	no	Private Adapters-Motherboard
Internal Network	Yes	Motherboard Private IP Address

Chapter 2

Specifications

Specifications

I would now like to present the specifications in two parts. The 1st part will deal with the OSI with my modified version to reflect a sub physical layer. The 2nd part sets the MAC address field parameters. Please also note I will presenting the lower level OSI layers 3rd and below.

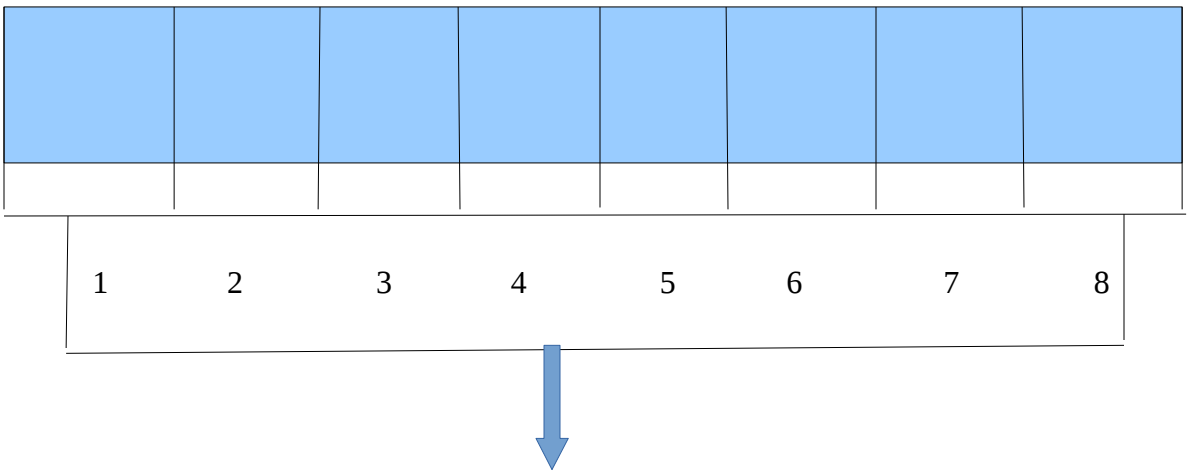
Modified Lower Level OSI Layer Lower level for 12228 System Interface

	8192 bits	12228 bits
IP layer 3rd layer Router Network Adapter Routable	192.168.1.1	192.168.1.2
Data link Layer – Frames Characters switch Non-Routable	64 bytes= 32 Characters	128 bytes= 64
Physical layer Physical medium Fiber Optic	8192 bits=64 bytes	12228 bits=128 bytes
Sub-Physical	6 volts = 8192 bits	9 volts= 12228 bits

Please note the Sub-Physical layer Voltage to bits The OSI 7 Stack layer generally regards this at the physical layer but the issue is the Dynamic usage of volts to bits instead of constant states so this is better represented by creating a sub-layer beneath the physical layer. Please note 3 volts produces 4096 bits per battery. Please also note physical medium is represented at the Physical layer so this layer has a broad classification.

I will now present the next set of linear motion specifications setting the MAC address field parameters.

8192 MAC Address Linear Field Specifications

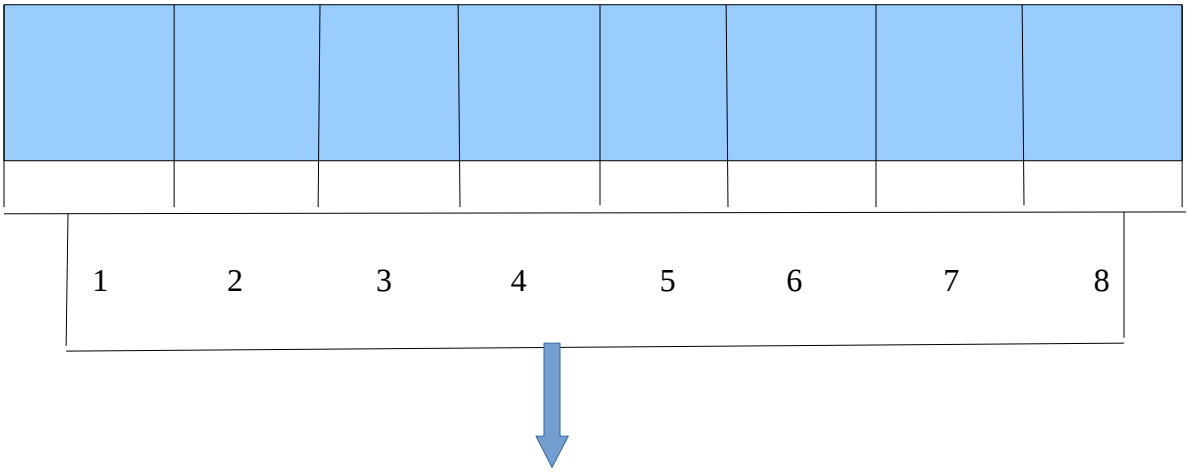


8 Fields 4 Characters

Linear Mac Address field parameters

1be5 f3sj 67mn yhjg okmn qafv jnbv jkge

12228 Linear MAC Address Specifications

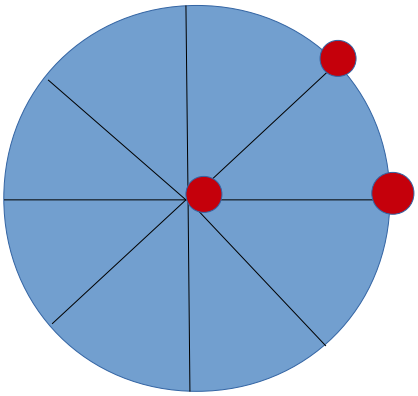


8 Fields 8 Characters

Mac Address field parameters

1be5fstz f3sj5tuc 67mnefgh yhjg89ol okmnytrc qafvsdfh jnbvolm7 jkge5ty7

12228 Curvature MAC Address Specifications



As stated recently in previous works, The implementation of curvature type motion coupled with Linear will now be implemented into System Bus Interface Designs.

Curvature Block Specifications

The Curvature Block specifications are the following:

12288 / 8 Areas = 1536 bits per block total 8 Areas of Space

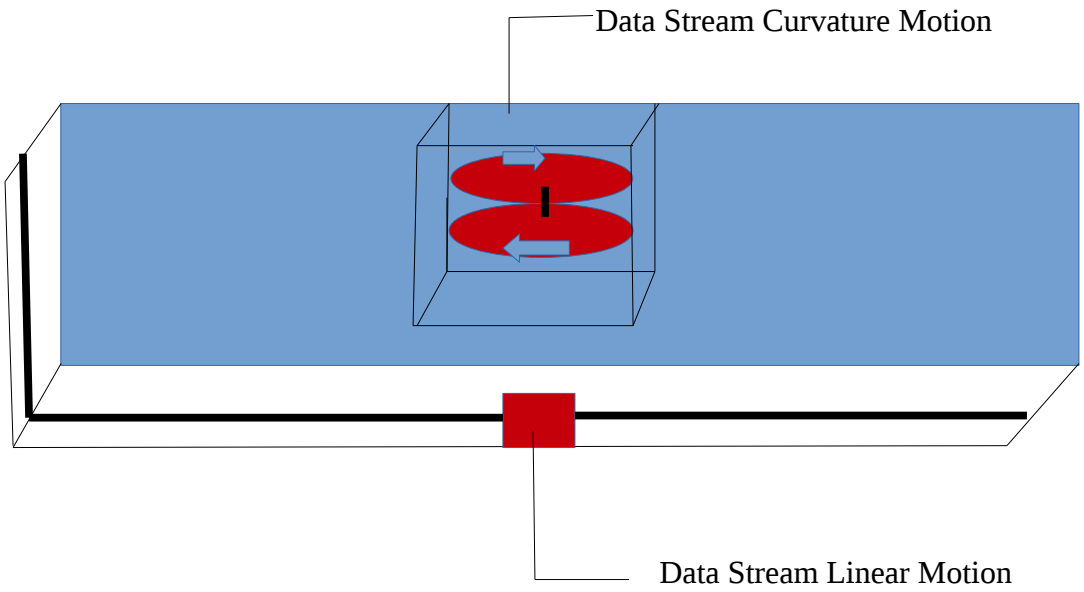
If you observe there are 3 points within each block if you divide this by 3

1536 / 3 = 512 you should have 512 bits within the block. The principal of time space formation can easily be completed by multiplying 512 * 3 = 1536 bits. This forms the 1536 bit block. If you wanted to secure this you can program a random selection choosing one of the 8 blocks. This is the Symmetrical or Constant Form. if you wish to take this further, consider forming the time and space by setting 2 of the 3 points and setting the last point 3rd point to a on or binary switch to on or off to check for conditions. This creates the Asymmetrical form of Energy Example below.

1536 / 2 =768 bits per block . This forms 768 bits per block 768 * 2 = 1536 This would be the asymmetrical type because 3 points for the time and space where the area of space has the first two points at 768 bits and the third point checks for either 1 = “on” or 0 = “off” thus a inequality has formed demonstrating a principal of energy being dynamic simply by employing a binary switch within the time and space within the Area. One final Example I can create a dynamic state within the 1536 bits per Area by having the binary switch as discussed also having one node point compressed 768/ 2 = 384 and the other point static at 768 bits This can be programmed as well for the End-User to select Symmetrical or Asymmetrical as described in the previous examples.

These examples are for the reader to better visualize it is possible to form more complex block schemes but this would lose sight of the idea of **employing curvature blocks within a 12288 bit system**.

Data Stream Hardware Block



This is a Internal Block that forms frames to packets. This also can be used to form Compression from within based on Linear and Curvature Motion. This is a device that is placed on the Interface.

This concludes the field specifications for the Lower Level OSI Networking layers and the mac addresses. A interesting point is if encapsulation occurs at the 2nd layer at the data link layer than would encryption be required if a binded private IP address is shelled within a Public address space across a unsecured Public Network. The reasoning is if the MAC addresses are shielded from roaming Networks wired and unwired than it stands to reason the only thing would be to authenticate the Receiver's address thus encrypting a link at a higher level on the OSI layer would prove to be a waste of time and energy because the tunnel is the Public Network space and within this shell is the Private IP address and within the IP address is a MAC address that during the process was encapsulated. To put it simply a shell within a shell this shows a two layer process dealing with assembling IP Packets hint most critical during TCP/IP and OSI Network operations..

This concludes chapter 2. I will now provide my final thoughts on this design in the next chapter.

Chapter 3

Final Thoughts

I have re-designed the 12228 Interface that is coupled with the Motherboard Design copyrighted Model Super Sonic 12 Motherboard- Design and 12288 Bit Architecture-2011 by Barry L. Crouse. I have attempted to show a different and unique designed coupled with a different process in relations to Networking and the OSI 7 stack layer. I believe that one size does not fit all because I can remember back in the 90's while gaining some exposure to Mid Size Servers that they were different than the PC based Architecture. After reviewing the Servers, I found most servers are based on PC based Architecture which I feel needs to be addressed. I have attempted to create new methods of packet delivery without the need for a application based encryption system by encapsulating the MAC addresses in this model there are four different methods and they are the following:

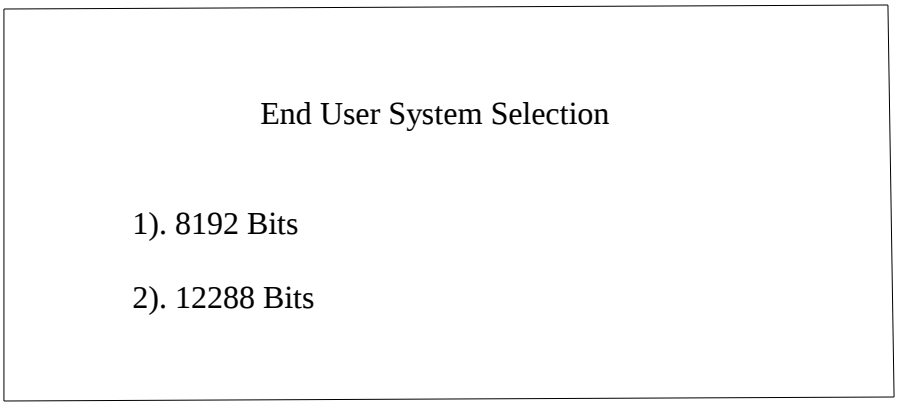
1). 8192 to 8192
2). 12228 to 12228
3). 8192 padded to 12228
4). 12228 compressed to 8192

This offers a variety of methods to deliver packets without the need for application based encryption within the OSI and the higher levels past the Networking IP routing protocols. I have also enhanced Mac address 2nd layer on the OSI stack by expanding the field and employing linear and curvature based motion thus the probability of a roaming Network hacking into a private based Network wired or UN-wired may not work out so well.

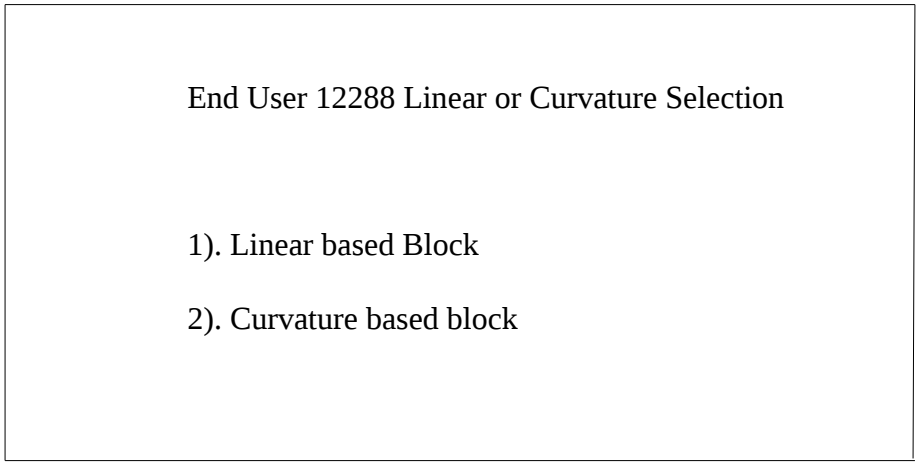
The process of delivering the packet is the following:

1). System Interface bios with 3 cmos batteries creating 2 boards of bios settings
2). System Interface uses 2 Non-Routable switches 8192 and 12228 encapsulated
3). Motherboard has 2 adapters attached to continue process of Encapsulation
4). The Encapsulated MAC address is binded to the Private Internal IP address
5). The tunnel is created to access the Public address space.
6). The private IP address is shelled within the tunnel Public address space.
7). The MAC address is shelled within the private IP address creating a 2 layer security approach to data security.

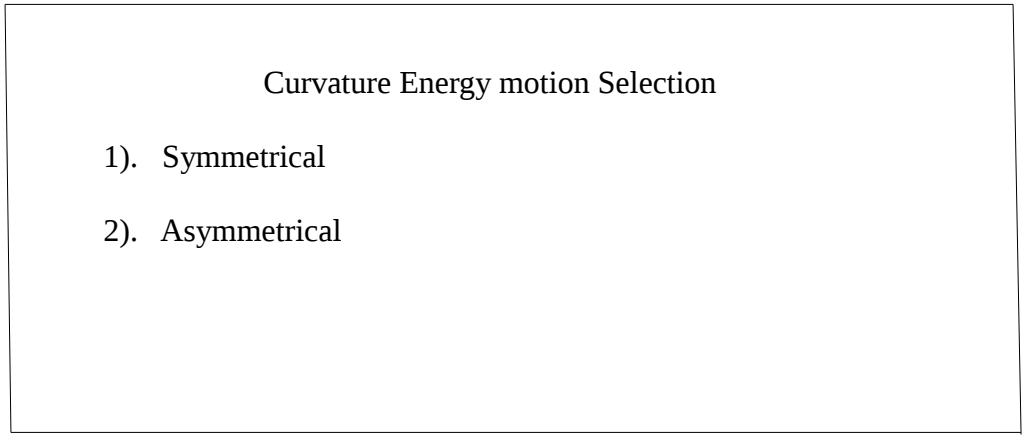
This creates a dynamic method of delivering data instead of creating constant states or links that decay. I have also created some menus as to how software can interface with the 12288 Interface itself as to better visualize and easier to understand. Please note this can be enhanced.



If user selects 12288 goto next menu
else
goto 8192 linear based blocks



If user selects Curvature based block goto next menu



The original Motherboard designed called for Encryption back in 2011 but with the new System Interface this will no longer be needed due to how the process of delivering data packets as described above.

I would like to take the time for thank each and everyone of you for reading this design concept coupled with the process involved.

Barry L. Crouse

Dated 10/26/2016

For more product information please goto the following website:

http://www.barrysscientificbasedproducts.com