

**Model SS24M-D**

**Model Super Sonic 24 Motherboard- Design and Private Public BIOS**

**By**

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## **Introduction**

Today is 08/07/2011 University Place, Washington. I would like to thank you for taking the time reading this scientific work. I have attempted to build upon the 15360 bit architecture and motherboard design by making and improving the design and employing some of the previous U.S. Copyrights registered for the purpose of taking theory's I have written and creating practical visual application to new theory's.

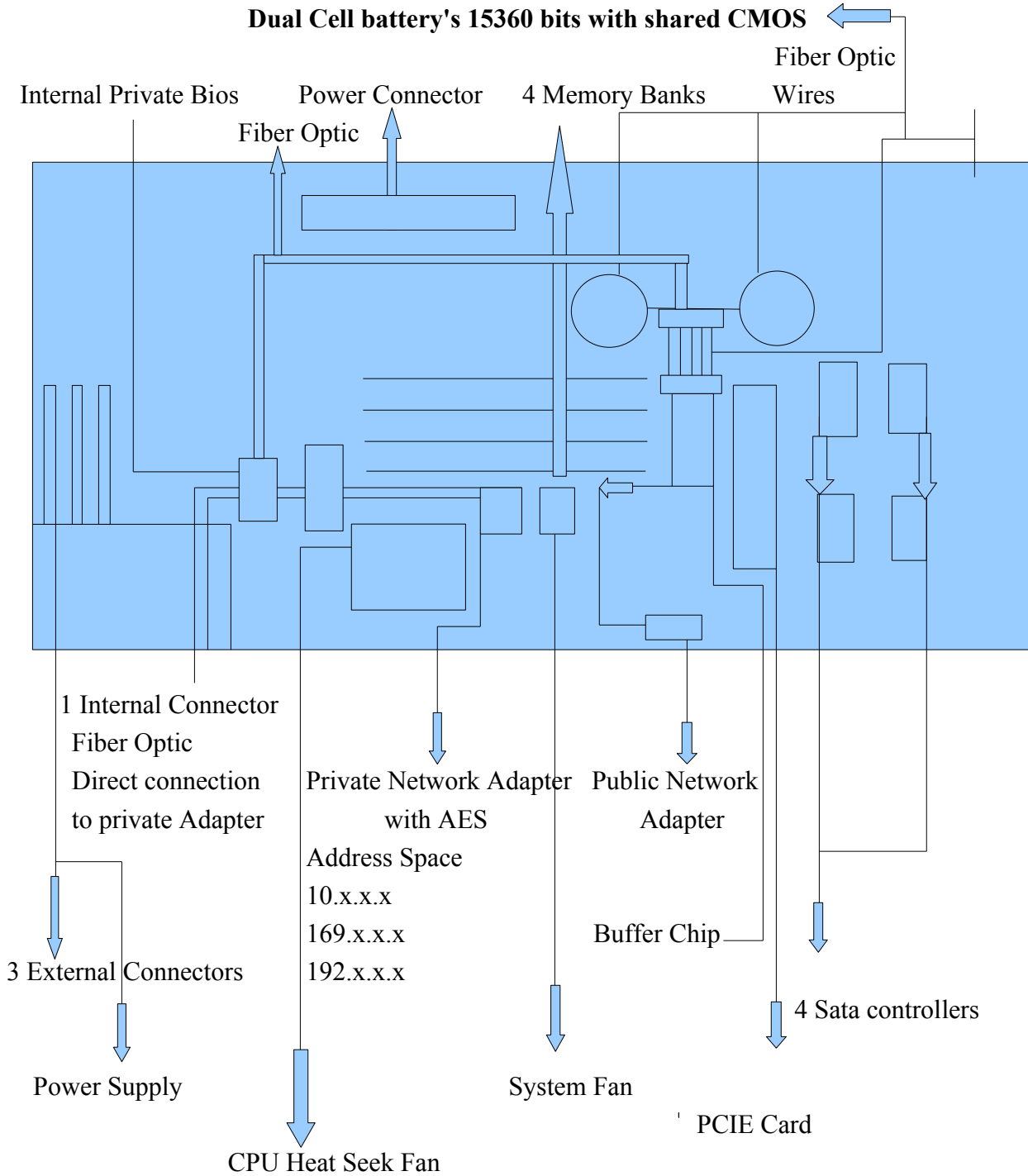
The Theory's I have written in my previous copyrights needed a answer as to how can a theory be made useful in everyday lives. Complex Theory, Design, and development is much like a ladder it takes gradual steps to arrive at a solution. I hope that if you have read my previous works you will find that in this paper some of the previous works being demonstrated such as Thoughts on Rotating Black Holes, OSI theoretical discussion, Visual Arts Equations, Temporal Spatial Equations, Why the Big Bang Theory is a Myth and other works as a example that answers the question above. I want to take the time to thank you once again for reading and studying this paper.

### **The New Design feature's include the following improvements**

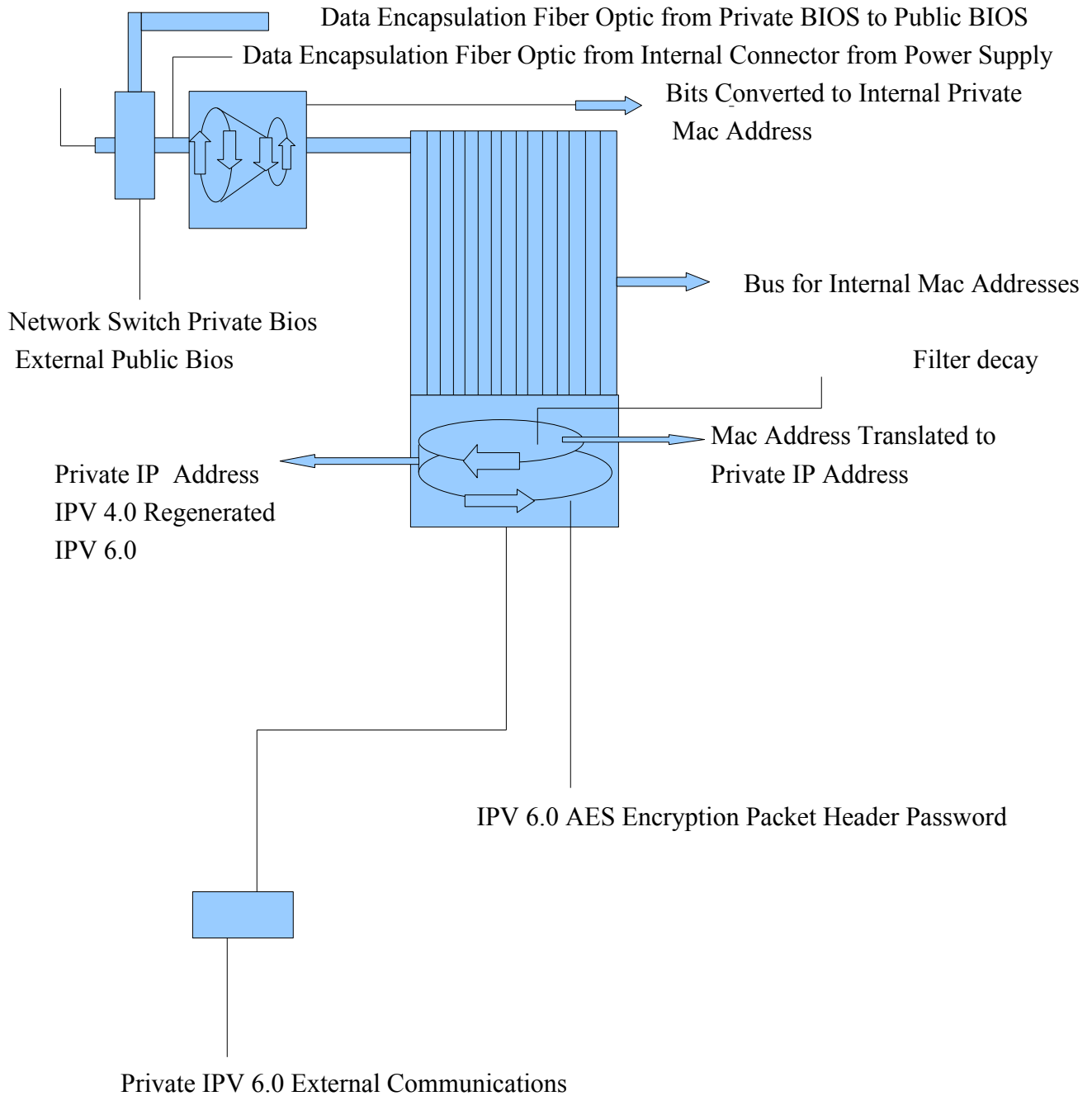
- 1). Private and Public BIOS
- 2). Data Switch from Private BIOS to Public BIOS Fiber Optic

# Model SS24 M-D

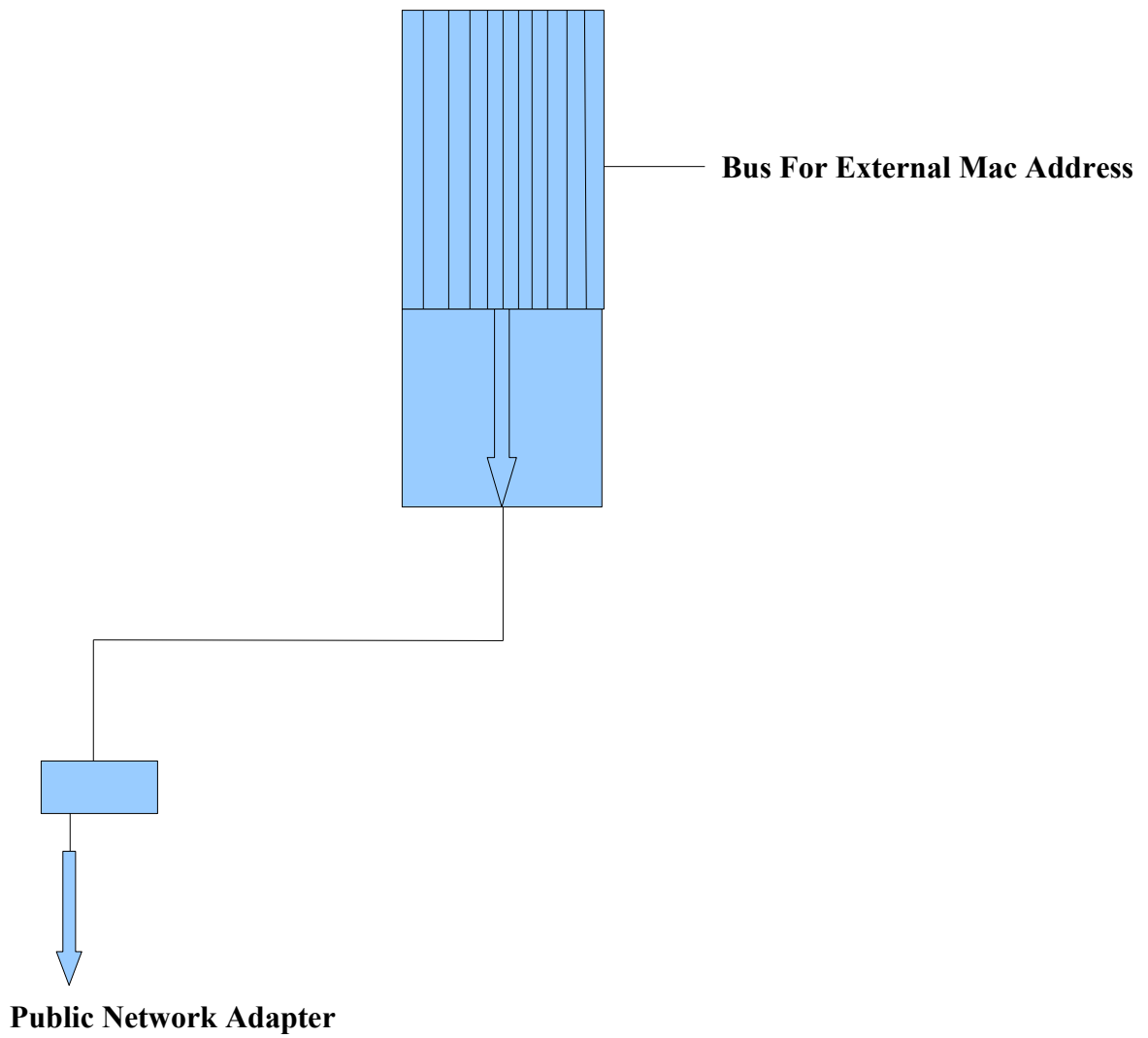
## Model Super Sonic 24 Motherboard- Design



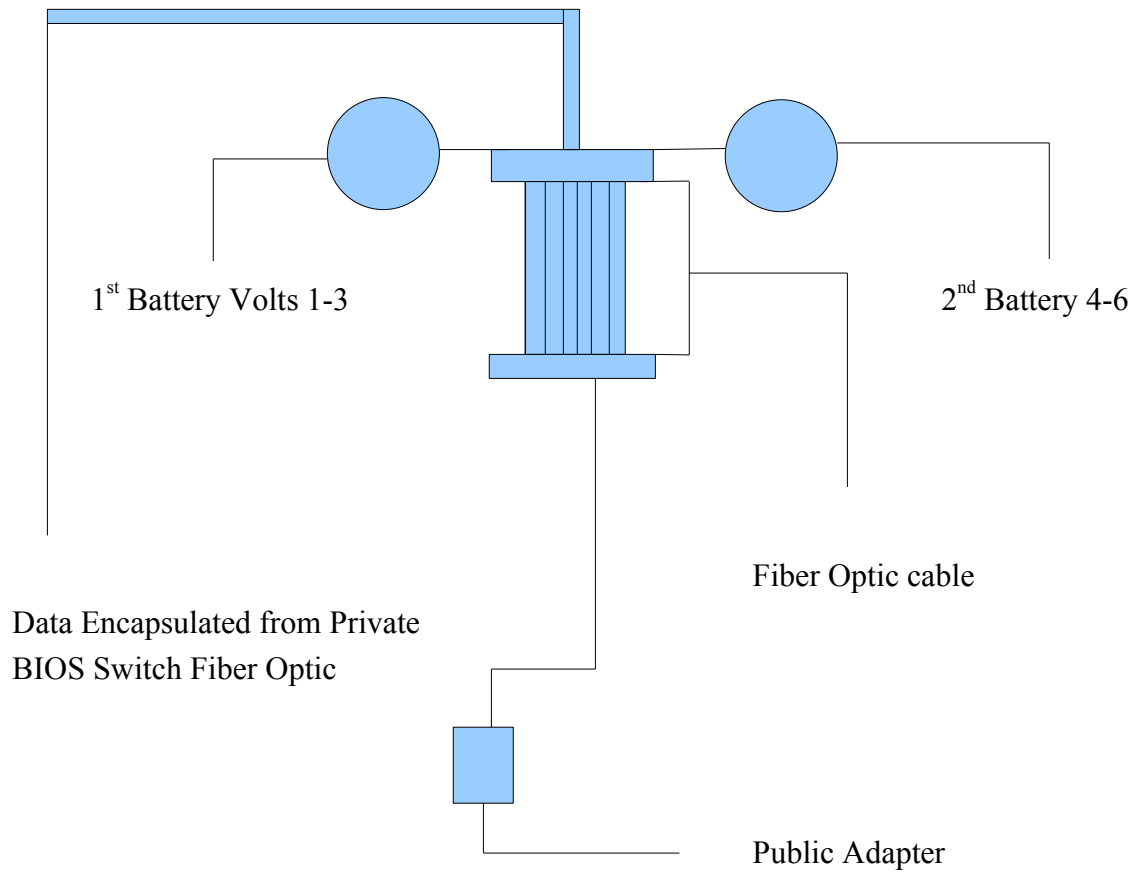
### Internal Private Switch



### Internal Public Switch IPV 4.0

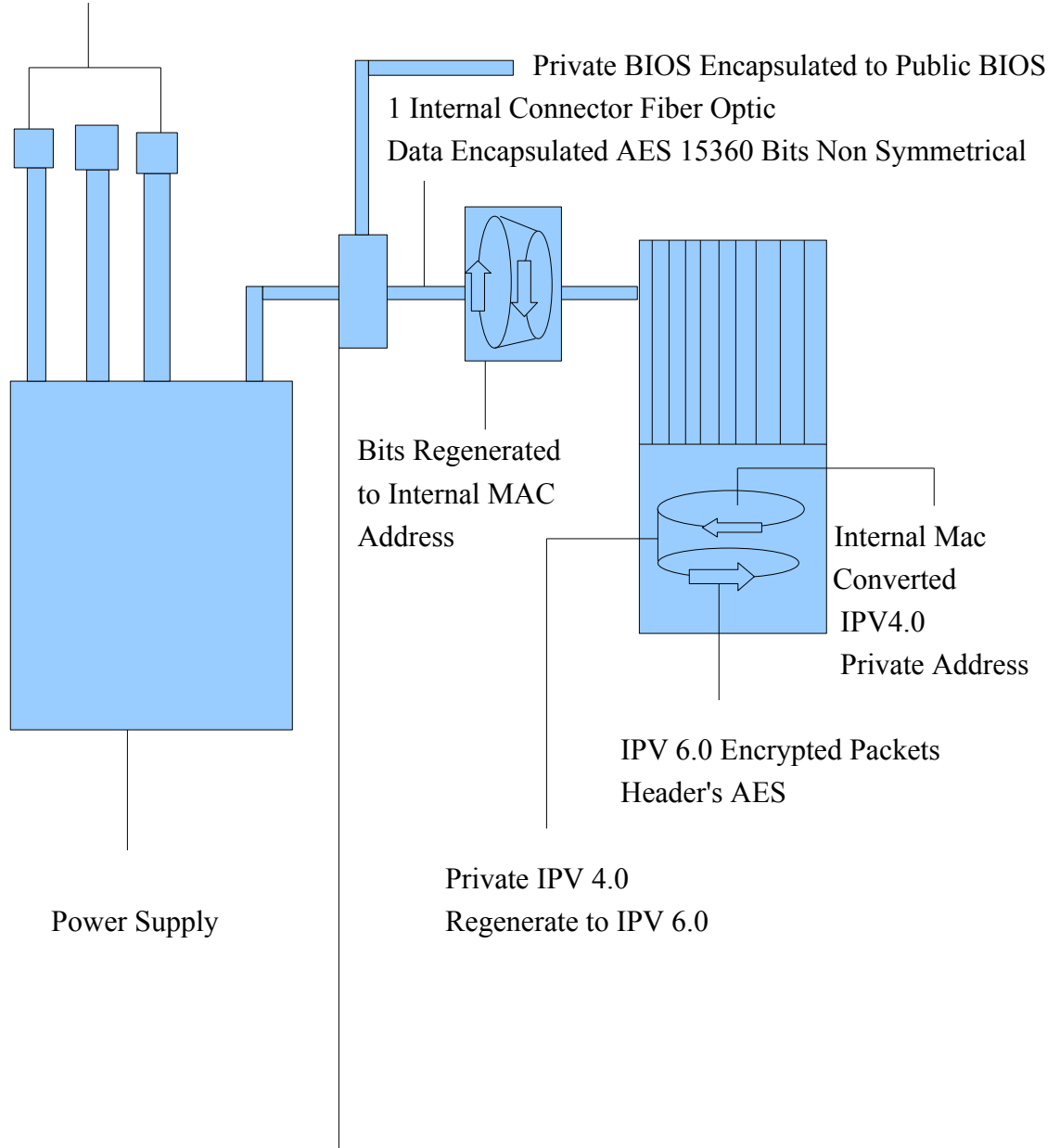


### Dual Cell battery's 15360 bits with shared External CMOS



## Power Supply

3 External Connector's standard Wire 3\* 4096 Bits Symmetrical total 12288



Power Supply

Data Switch Determines Private or Public BIOS

## **Internal Voltage to Bit Conversion Notes**

The Power Supply has a Fiber Optic Cable that employs Data Encapsulation thus it prevents less bit decay and promotes data security in a Internal Environment. The next step is it goes to a Data Switch requesting either a Private or a Public Bios. If it goes to the Public Bios the Data is encapsulated via Fiber Optic to prevent external environmental corruption it then proceeds with normal symmetrical processing. If it goes to the private Bios it goes through a Rotating Black hole taking charged particles and Regenerating from Bits to a Internal Mac Address this employs Non Symmetrical processing. In previous works, Temporal Spatial Equations I proposed having data encapsulated to promote energy efficiency and effectiveness this allows bits from being exposed to External Environments that corrupt data for whatever reasons. The Internal Private Address allows for better usage of bits and I am able to deliver 15360 bits in a efficient manner compared to the External Power connectors utilizing 4096 bits per connector. The Private Internal switch allows time and motion to accelerate by saving wasted motion in the form of Packet delivery. A simple question would be which would be a better usage of energy 3 external connectors utilizing 4096 bits each for a total of 12228 or a Internal Data Encapsulated connector that utilizes 1 private switch at 15360 bits ? The obvious answer is the Internal Connector Data Encapsulated. Please note by showing this kind of Energy I have shown that time and space are Dynamic not static.

On another note I have attempted to provide a choice to load either a Private or Public Bios thus the End-User has the choice to determine which one they want. A good application for this would be a Public Bios would work well with the Social Network but a scientific exchange of Information would work in a Private Bios setting at the same time promoting Social awareness networks with Privacy and Security by basing it on consumer choices..



## External Power Connector's Voltage to Bits Chart

### 1<sup>st</sup> Battery Voltage/Bits produced

|                      |      |
|----------------------|------|
| 1 <sup>st</sup> Volt | 1024 |
| 2 <sup>nd</sup> Volt | 2048 |
| 3 <sup>rd</sup> Volt | 4096 |

### 2<sup>nd</sup> Battery Voltage/Bits Produced

|                               |                                   |
|-------------------------------|-----------------------------------|
| 4 <sup>th</sup> Volt          | 8192                              |
| 5 <sup>th</sup> Volt          | 12288                             |
| 6 <sup>th</sup> Volt Reserved | for Reallocation and Distribution |

This is a conversion chart to show how many volts are to be converted from volts to bits. In my OSI Theoretical discussion I proposed a sub Physical layer at the lower stack of the OSI Please view the following

Network Layer frames assembled to packets IP Routing begins here  
Data Link Layer Bytes into Frames Bridging begins here Non- Rout able  
Physical Layer Bits into Bytes  
Sub-Physical Voltage into Bits  
Atomic Sub Particle layer Electrons, Proton Nucleus

## **Summary of New Features to 15360 Bit encryption**

Today is 08/06/2011 University Place, Washington. I would like to go over my new board design with the new features that builds upon the 15360 Motherboard design and Architecture.

After reviewing the design diagrams, You will notice that I have added new design features in my 15360 bit motherboard design and architecture. Some of the new features are the following

1. Separate Private and Public Bios to promote privacy and security along with the ability to have access to Social Networks along with Energy Efficiency.
- 2). Data is Encapsulated via Fiber Optic Wire from the Private Bios to the Public Bios promoting Energy efficiency and effectiveness coupled with filtering out External Environmental pollution concerns.
- 3). Consumers have choices as to what settings are needed to access the outside world by either having less security via Public Bios or strict security utilizing Private Bios through a Data switch. This also promotes Symmetrical and Non Symmetrical processing promoting Dynamic Environments.

I have provided a brief summary and now I would like to go into greater detail about the new design which is entitled SS24M-D Motherboard design meaning Super Sonic 24 Motherboard Design which is the 4<sup>th</sup> development to enhance privacy and security along with Energy Efficiency

The 1<sup>st</sup> Design Feature Separates Internal and External Bios settings when the consumer chooses Public the Data is Encapsulated from the Private Bios via Fiber Optic Wire and delivered to the Public Bios where the settings go through a normal PC processing procedure. If the consumer chooses Private Bios it goes through a Non Symmetrical processing namely 15360 bit IT security procedures. Data is Encapsulated and Bits are processed into a Internal Mac and converts into Private IPV4.0 addresses than it is regenerated into IPV 6.0 addresses with AES encrypted packets and header's. Bit filtering begins when the consumer allows for Private IP processing through the Rotating Black hole thus the process of Regeneration and Decay begins at the 1<sup>st</sup> event horizon when the consumer chooses Private Bios settings.

The 2<sup>nd</sup> Design Feature is the Fiber Optic cable Data Encapsulated from the Private Bios to the Public Bios this promotes Energy efficiency and filters out External Environmental pollution such as Crosstalk, Noise, and other signaling Interference issues. On another note packet delivery is much more private and secured.

## Testing and Experimental Notes

The following was tested from a software standpoint and showed very little problems.

1. Certificate of Authority E-mail Certificate 4096 Bits with 3 sub key encryption 1<sup>st</sup> sub key 4096 2<sup>nd</sup> sub key 4096 and 3<sup>rd</sup> sub key 3072 total bits 15360 bits creation of the certificate and sub keys tested okay and was able to send email and encryption to my trusted user which is my wife's E-mail account. The key was published. I produced another Certificate using the following parameters 1 Digital Signature 4096 2 sub keys 4096 total 8192 bits 1 sub key 2048 bits for a total of 14336 bits
- 2). Using Key Rings was able to implement MD-5 IP Packet Header Protection problem here is the uncooperative attitude when dealing with Data Centers and privacy. This is at best a 50 percent chance of success. When it is utilized this becomes a effective tool in sending secured E-mail and trusted web site information and validation.
- 3). I tested Ipv4 with link local Ipv6 limited and Automatic in scope this worked sometimes when they are combined.
- 4). SSH I created a RSA 8205 bit secure shell. This worked 1 time but was not tested again because of the Data Centers to let End User clients exercise the right to privacy also when checking Email client accounts for Authentication the one they allowed was Clear text or Login which

means a IP packet can be Re-directed and corrupted which is kind of baffling to not secure End-User Clients IP packets and allow for these kind of actions to continue. A Possible work around

- 5). I attempted to avoid applications that insist on total control dealing with file and property rights and choosing applications that will allow MD-5 or AES Authentication methods to be utilized.
  
- 6). This would mean applications that have a automation process will show to be ineffective while applications that require customization will fare better.

In conclusion, I have attempted to build upon my 15360 bit IT Architecture and Motherboard design by utilizing separating Network switches which allows for Intelligent choice as to whether to utilize a Private or Public network switch thereby allowing bits to either Regenerate or decay which I first proposed in my previous U.S. Copyrights. I have attempted to Encapsulate Data which should allow for energy to be better harnessed and better utilized than to incur more loss of energy. The Fiber optic cable going from the private Bios promotes Energy Efficiency and Effectiveness and allows for bits to be processed in a Internal Environment protecting it from External Environmental conditions such as Public address spaces that contain Virus attachments and other questionable activity. The upgrades as proposed is a gradual improvement of existing IT design, Architecture, and or implementation on a industrial scale or commonly called Economy of scales. I would like to provide a Pseudo code that could be used when a PC boots up.

### **Pseudo Code for Initial Boot PC process**

A = Private Bios

B = Public Bios

Default = Public Bios Default

If A

then

Goto Private BIOS processing

Else

If B

then

Goto Public Bios processing

Else

Goto Public Bios

### **Private Bios Processing**

Non Symmetrical Processing begins

Bits are filtered and decay begins at the 1<sup>st</sup> Event

Bits are processed into Bytes which are converted into Internal Mac addresses

Internal Mac address are converted into Private IPV 4.0 addresses

2<sup>nd</sup> Event Private IPV 4.0 are Regenerated into IPV 6.0 with Packet Encryption and Headers using AES

Packets ready for Private communications employing Privacy and Security

### **Public Bios processing**

Symmetrical processing begins

Data Encapsulated from Private BIOS via Fiber Optic

Public BIOS settings loaded using IPV 4.0 utilizing Public Switch.

End

This is a sample code and Instructions on how this can be implemented. The idea here is not to write a application program but show how a system can employ Symmetrical and Non Symmetrical processing at Initial boot time.

## **Conclusion and Summary**

The objective accomplished was to provide practical application to the previous U.S. Copyrights written because I believe it is not enough to write a theory and not provide a useful application to the theory proposed some examples are thoughts on Rotating Black holes, OSI theoretical discussion, Linear Cryptographic in Real time mode, Temporal Spatial Equations and Dynamic usage of Time and Space, and Why the Big Bang Theory is a Myth. If you are interested in other works that incorporate Physics, Mathematics, and Computers, Please visit my web site below.

Dated 08/07/2011

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