Introduction

Model SS6M-D

Model Super Sonic 12 Motherboard- Design and 12288 Bit Architecture

By

Barry L. Crouse

Today is 04/06/2011 University Place, Washington. I would like to thank you for taking the time reading this scientific work. I have attempted to build upon the 8192 bit architecture and motherboard design by making and improving the design and employing some of the previous U.S. Copyrights registered for the purpose of taking theory's I have written and creating practical application to new theory's.

The Theory's I have written in my previous copyrights needed a answer as to how can a theory be made useful in everyday lives. Complex Theory, Design, and development is much like a ladder it takes gradual steps to arrive at a solution. I hope that if you have read my previous works you will find that in this paper some of the previous works being demonstrated such as Thoughts on Rotating Black Holes, OSI theoretical discussion, and other works as a example. I want to take the time to thank you once again for reading and studying this paper.

The Next Design feature's will include the following improvements

1). Power Connectors
2). Power Supply
3). BUS for MAC address
4). Atomic Sub Particle layer

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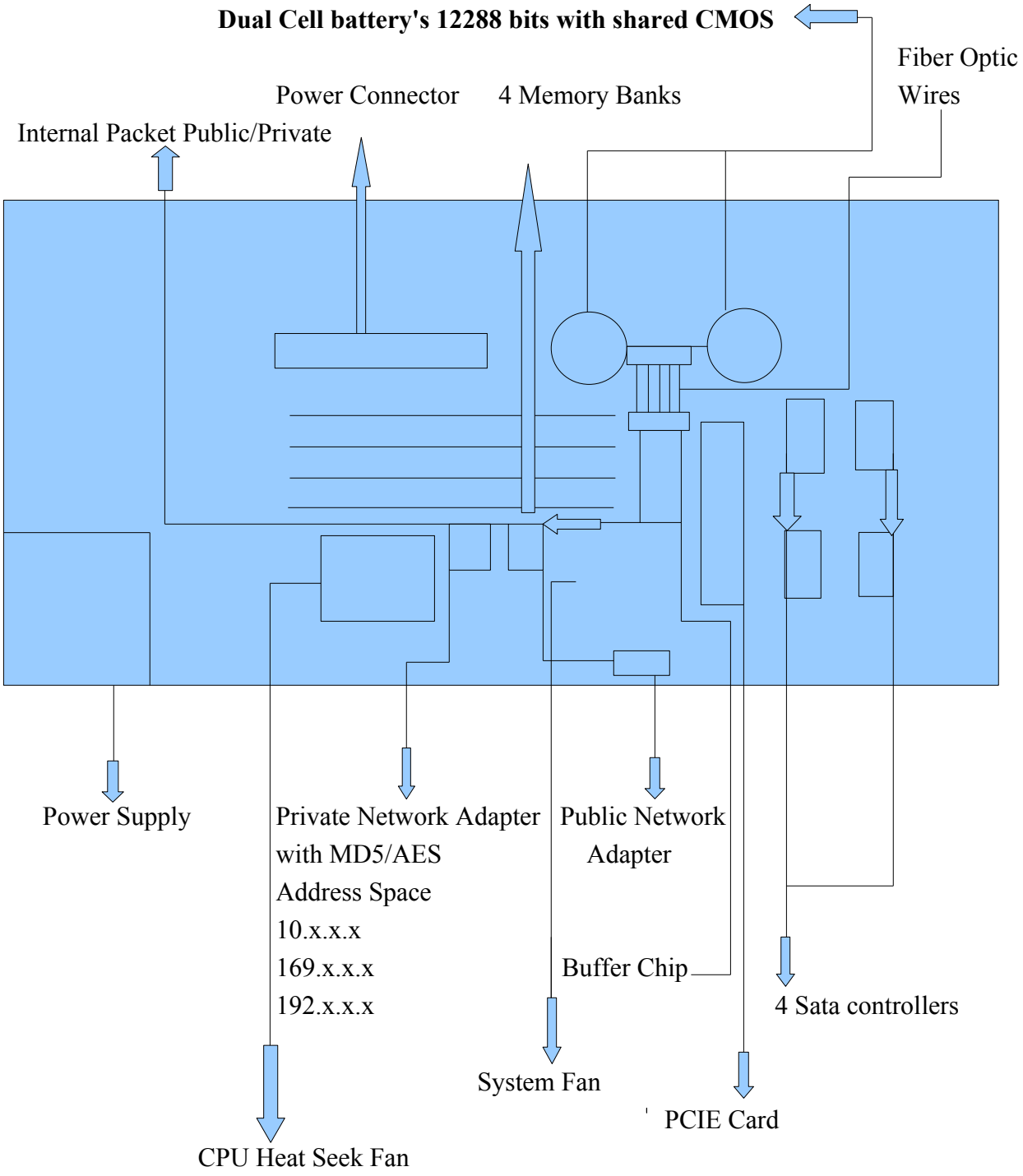
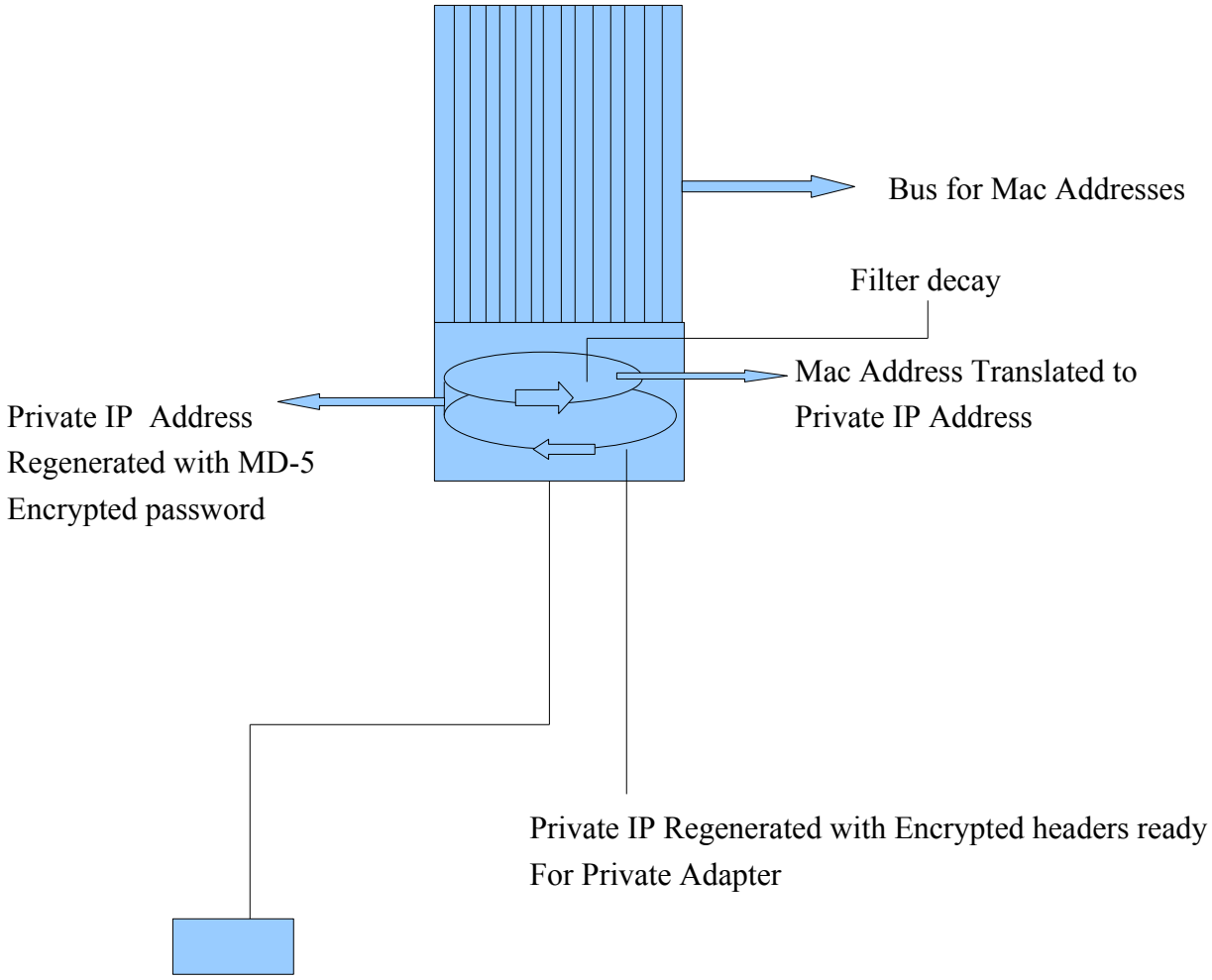
Model SS6M-D

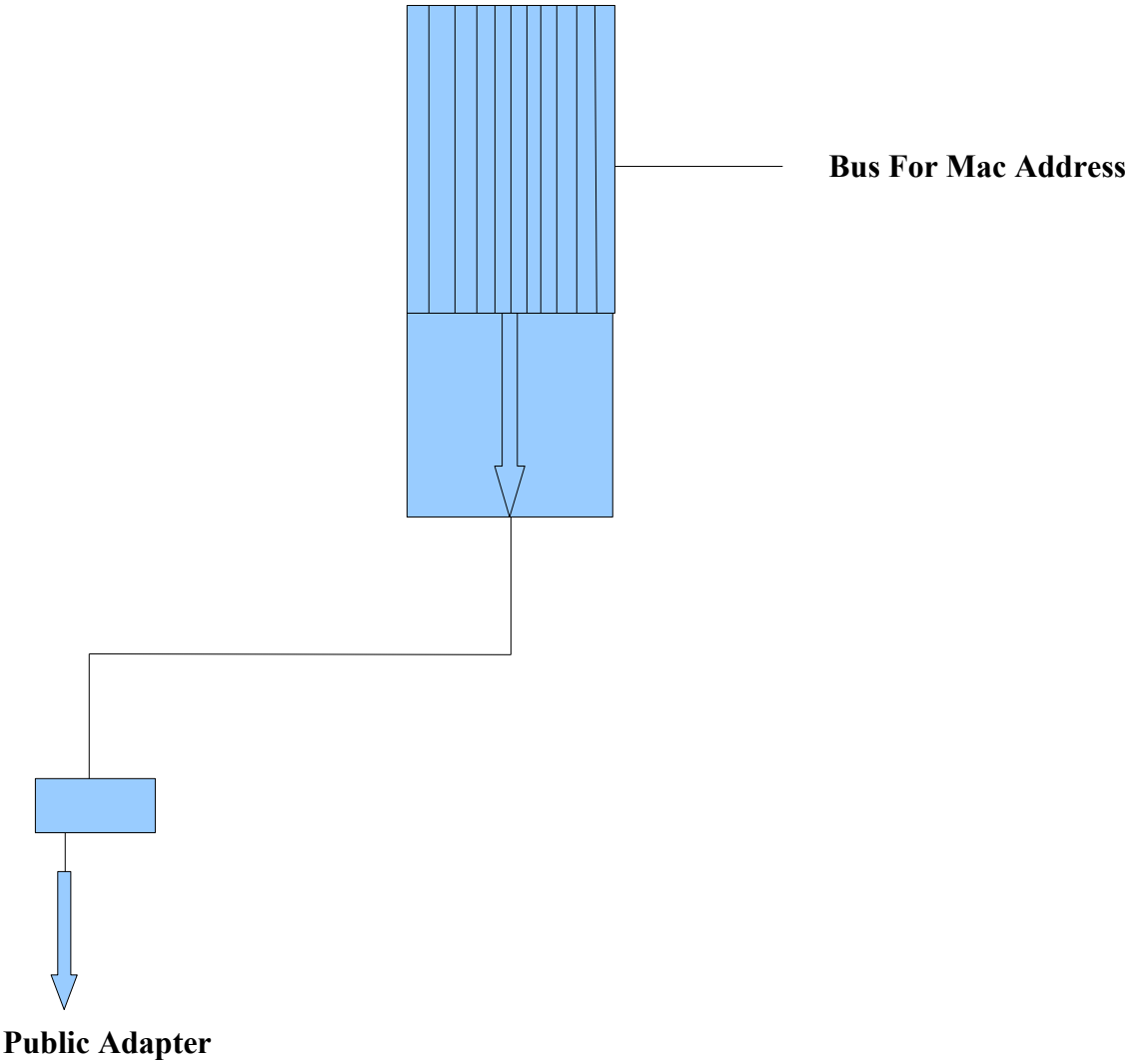
Model Super Sonic 12 Motherboard- Design



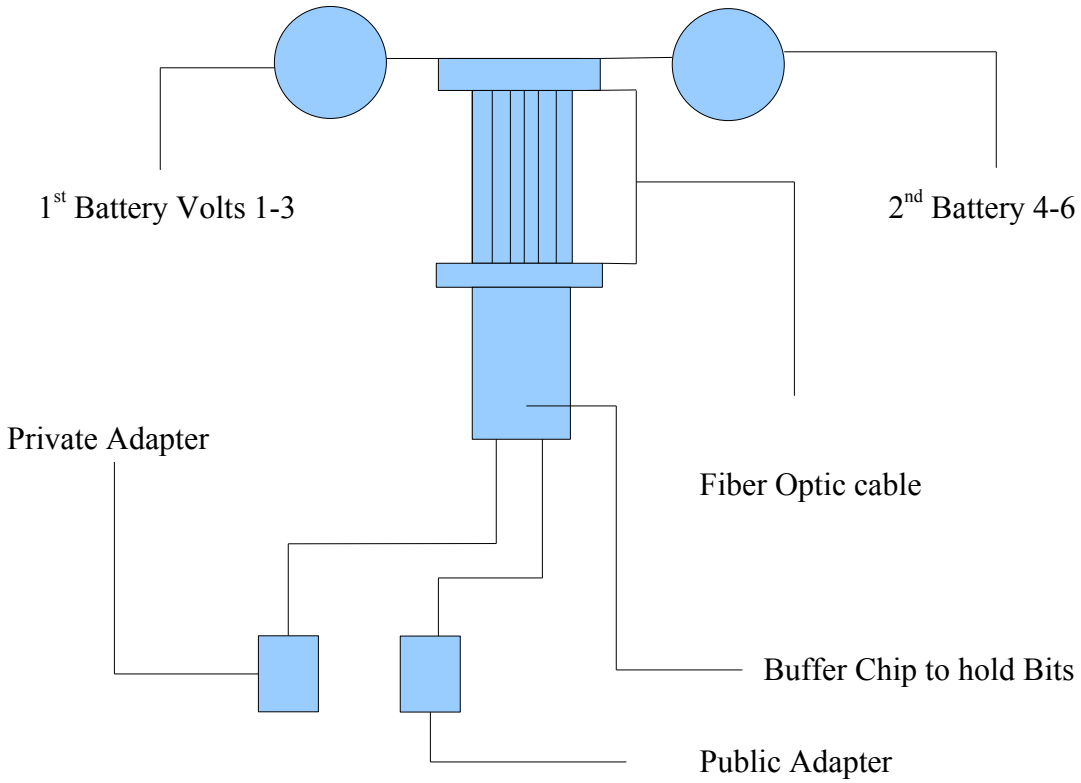
Internal Private Switch



Internal Public Switch



Dual Cell battery's 12288 bits with shared CMOS



Voltage to Bits Chart

1st Battery Voltage/Bits produced

1st Volt	1024
2nd Volt	2048
3rd Volt	4096

2nd Battery Voltage/Bits Produced

4th Volt	8192
5th Volt	12288

6th Volt Reserved for Reallocation and Distribution

This is a conversion chart to show how many volts are to be converted from volts to bits. In my OSI Theoretical discussion I proposed a sub Physical layer at the lower stack of the OSI Please view the following

Network Layer frames assembled to packets IP Routing begins here
Data Link Layer Bytes into Frames Bridging begins here Non- Routable
Physical Layer Bits into Bytes
Sub-Physical Voltage into Bits
Atomic Sub Particle layer Electrons, Proton Nucleus

Summary of New Features to 12288 Bit encryption

Today is 04/04/2011 University Place, Washington. I would like to go over my new board design with the new features that builds upon the 8192 Motherboard design and Architecture.

After reviewing the design diagrams, You will notice that I have added new design features in my 8192 bit motherboard design and architecture. Some of the new features are the following

1. The Share CMOS 6 volt battery has a fiber Optic cable that allows more voltage to be pushed through the wire.

2). The cable has a attached buffer bus chip to allow for energy to be regenerated when system throughput and bottlenecks becomes excessive

3). The Private adapter allows IP headers to become encrypted using MD-5 and AES methods that are cracked only by mainframes or brute force attacks.

4). The Internal Private Network Switch creates a bridge for the private adapter allowing the MAC address to translate and regenerate into private IP addresses with encrypted headers.

5). The Public Network switch allows for Public IP addresses to be processed in regular fashion.

I have provided a brief summary and now I would like to go into greater detail about the new design which is entitled SS6M-D Motherboard design meaning Super Sonic 6 Motherboard Design which is the 2nd development to enhance privacy and security of End User Clients.

The 1st new Design feature calls for the CMOS battery's to share resources processing at 5 volts 12288 bits. The problem is not processing the bits at this level but how to achieve energy efficiency and not have as much bit decay. The solution I think would be to create a Fiber Optic cable between the two battery's this will allow bits to be processed at a faster rate or in this case pushing more bits through the wires.

The 2nd Design feature allows for the bits to stay in a buffer if system bottlenecks occurs.

The 3rd Design feature has a Private and Public Switch. The Private Internal Network switch allows MAC addresses to be regenerated into Reserved Private IP addresses with encrypted IP headers using MD-5 or AES methods. Also another feature is a filter for bit decay is place on the Rotating Black hole to allow for bit decay to be done so that energy can either Regenerate or decay in a discreet manner. The Public Network Switch does not allow for encrypted IP headers thus regular processing as done here.

I have attempted to provide a description of the new features and modifications of my previous design. I have chosen not to update the bus with Fiber Optic cables at this time because a determination of how may bits can be pushed through the bus will have to be reviewed carefully.

Testing and Experimental Notes

The following was tested from a software standpoint and showed very little problems.

1. Certificate of Authority E-mail Certificate 4096 Bits with 2 sub key encryption 4096 total bits 12288 bits creation of the certificate and sub keys tested okay and was able to send email and encryption to my trusted user which is my wife's E-mail account. The key was published

2). Using Key Rings was able to implement MD-5 IP Packet Header Protection problem here is the uncooperative attitude when dealing with Data Centers and privacy. This is at best a 50 percent chance of success. When it is utilized this becomes a effective tool in sending secured E-mail and trusted web site information and validation.

3). I tested Ipv4 with link local Ipv6 limited in scope this worked okay especially when setting the firewall to TCP Reliable packets. I could not obtain automatic addresses when tested

4). SSH I created a RSA 8192 bit secure shell. This worked 1 time but was not tested again because of the Data Centers to let End User clients exercise the right to privacy also when checking Email client accounts for Authentication the one they allowed was Clear text or Login which means a IP packet can be Re-directed and corrupted which is kind of baffling to to not secure End-User Clients IP packets and allow for these kind of actions to continue. A Possible work around is to avoid applications that insist on total control dealing with file and property rights and choosing applications that will allow MD-5 or AES Authentication methods to be utilized.

5). This would mean applications that have a automation process will show to be ineffective while applications that require customization will fare better.

In conclusion, I have attempted to build upon my 8192 bit IT Architecture and Motherboard design by utilizing Internal Network switches which allows for Intelligent choice as to whether to utilize a Private or Public network switch thereby allowing bits to either Regenerate or decay which I first proposed in my previous U.S. Copyrights. I have attempted to create a buffer which should allow for energy to be better harnessed and better utilized than to incur more loss of energy. The Fiber optic cable going from the CMOS battery's to the BIT buffer chip allows for bits to be processed in a similar process such as printer que's also it avoids system bottleneck occurrences. I did not want to redesign the bus because more research will have to be done from a hardware and software point. The upgrades as proposed is a gradual improvement of existing IT design, Architecture, and or implementation and should not be that hard for Computer Motherboard designers to implement on a industrial scale or commonly called Economy of scales.

The objective accomplished was to provide practical application to the previous U.S. Copyrights written because I believe it is not enough to write a theory and not provide a useful application to the theory proposed some examples are thoughts on Rotating Black holes, OSI theoretical discussion, Linear Cryptographic in Real time mode and other copyrights

Dated 04/06/2011

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