# Barrys SS-65-1.2-B Revision  Motherboard Design

**by**

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## Introduction

Thank you for taking the time in reading this Scientific Work. I will be doing things a little differently in this paper mainly placing more detail and emphasis on my Memory Chip design complete with specs, charts and a subroutine program within the Main Module also I will be demonstrating the idea of **Barrys Non-Relativity Theory** . On another note, This work is based on Intelligent Design. If you are a secular scientist, This work will probably not be for you.

This work will use a lot of Visual Designs along with Charts and specs to promote previous ideas and concepts along with creating Logic Gateways and paths. Chapter 3 has a subroutine that creates a memory table module.

I will be providing enhancements and more details pertaining to memory chips emphasizing fault tolerances, memory optimization and allocation, along with Enhanced data Security methods. Please note Memory Chips will use Titanium instead of alloys for better heat tolernces.

I will also show how time and space become mote or irrelevant by providing a concept idea or principle that I discussed in previous works see Network Topology $18^{th}$ and $20^{th}$ higher order polygons and designs search engine keywords Barry Crouse Network Topology Design.

Thank you for reading this work!

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# Chapter 1

# Visual Design

**Solar to Mechanical Energy 1-B**

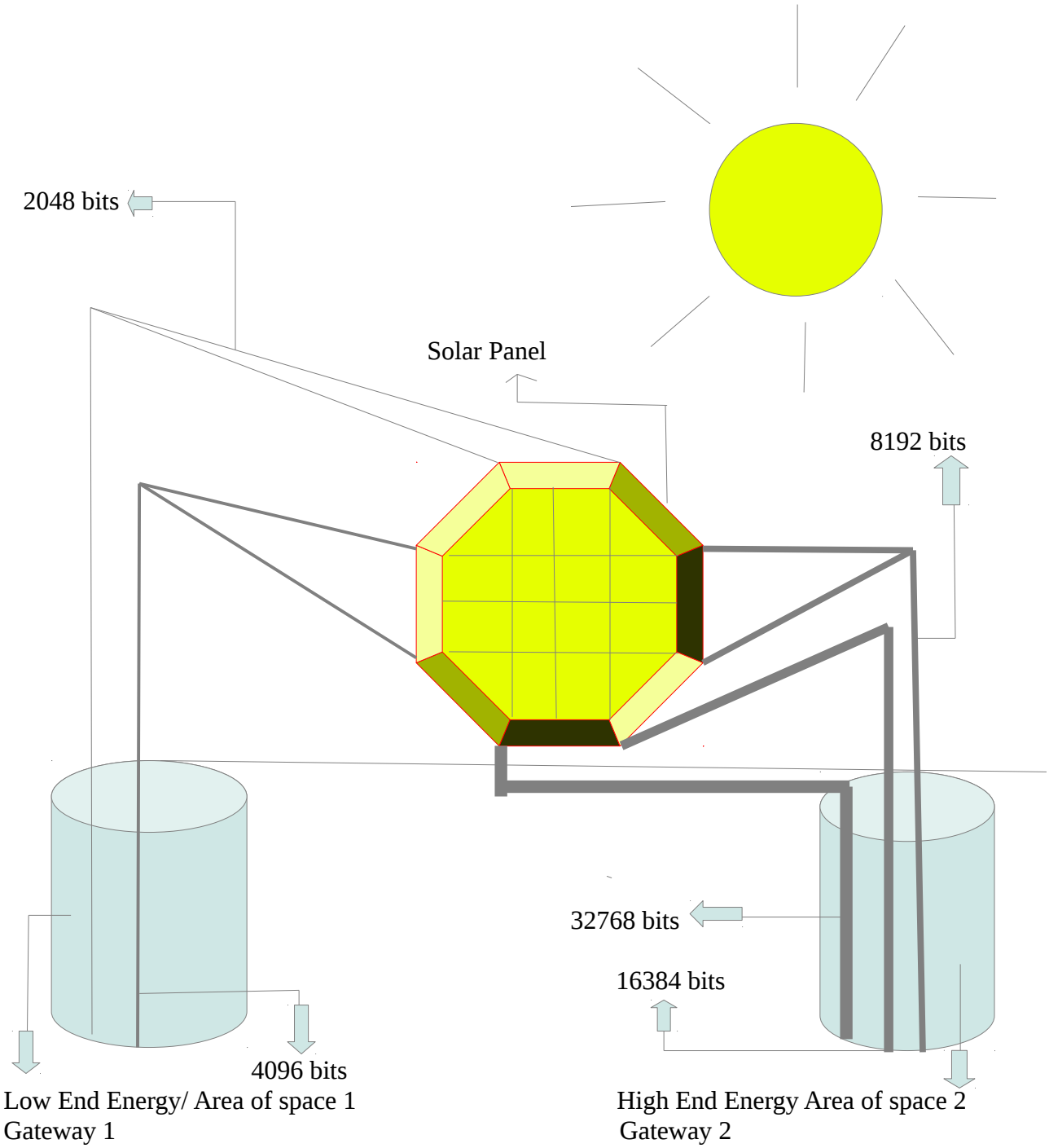
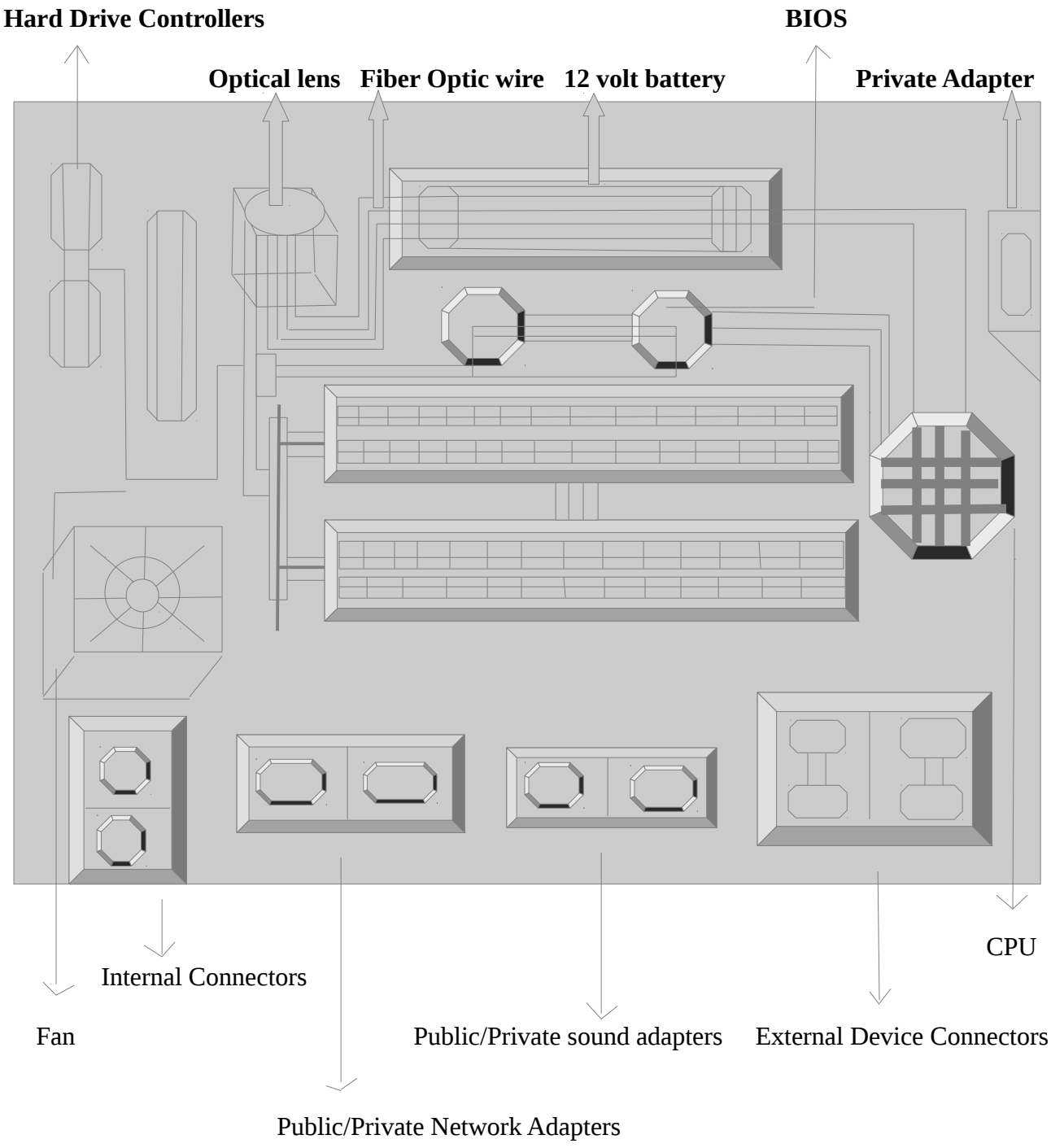


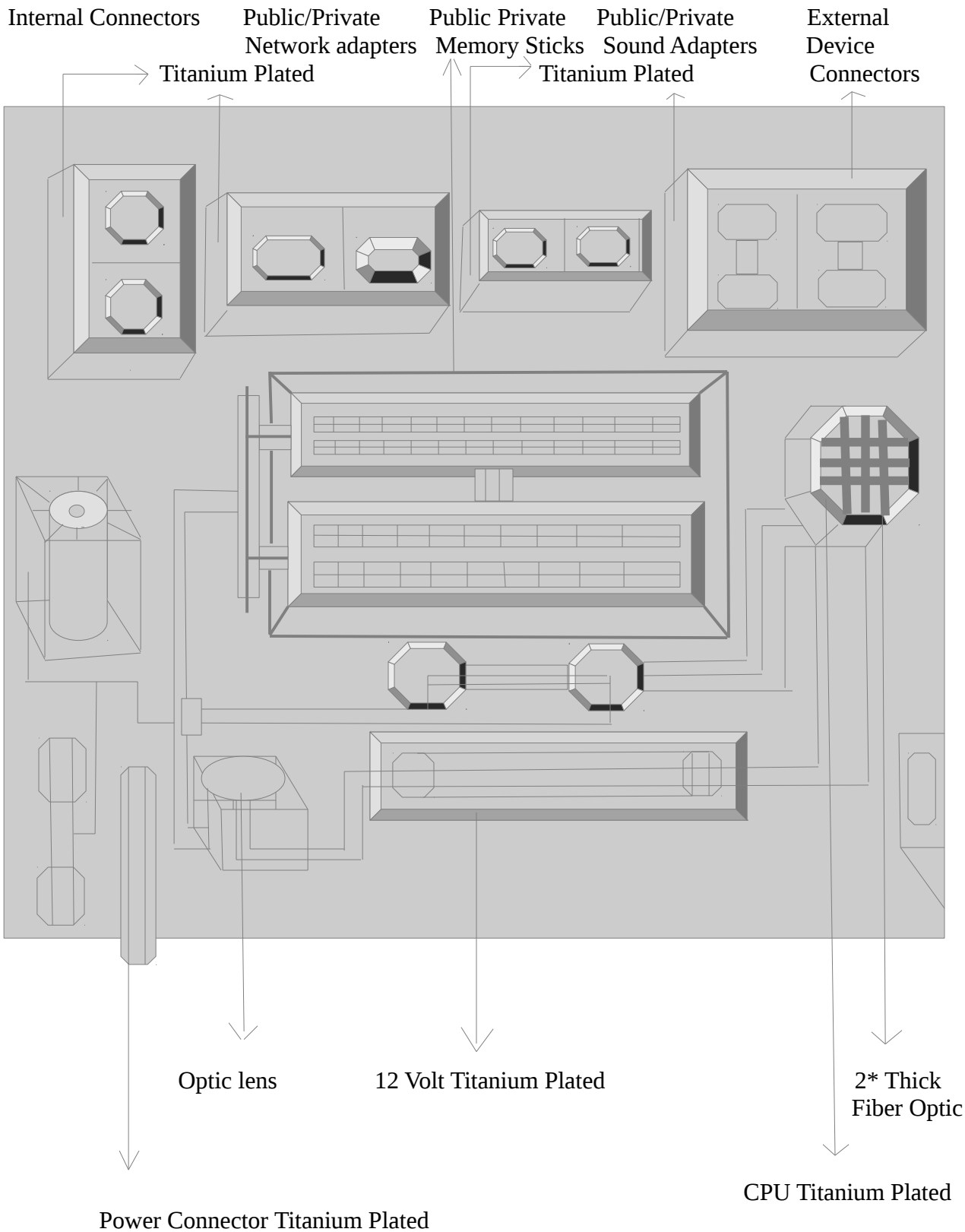
**Table of Light to Mechanical Energy Conversion 2-A**

| # of wires | Total Bits | Material |
|---|---|---|
| 2 | 2048 | Copper |
| 2 | 4096 | Copper |
| 1 | 8192 | Thin Fiber Optic |
| 1 | 16384 | Thick Fiber Optic |
| 1 | 32768 | 2* Thick Fiber Optic |

**Model Super Sonic 65 Motherboard- Design 3-B rev 1.2**

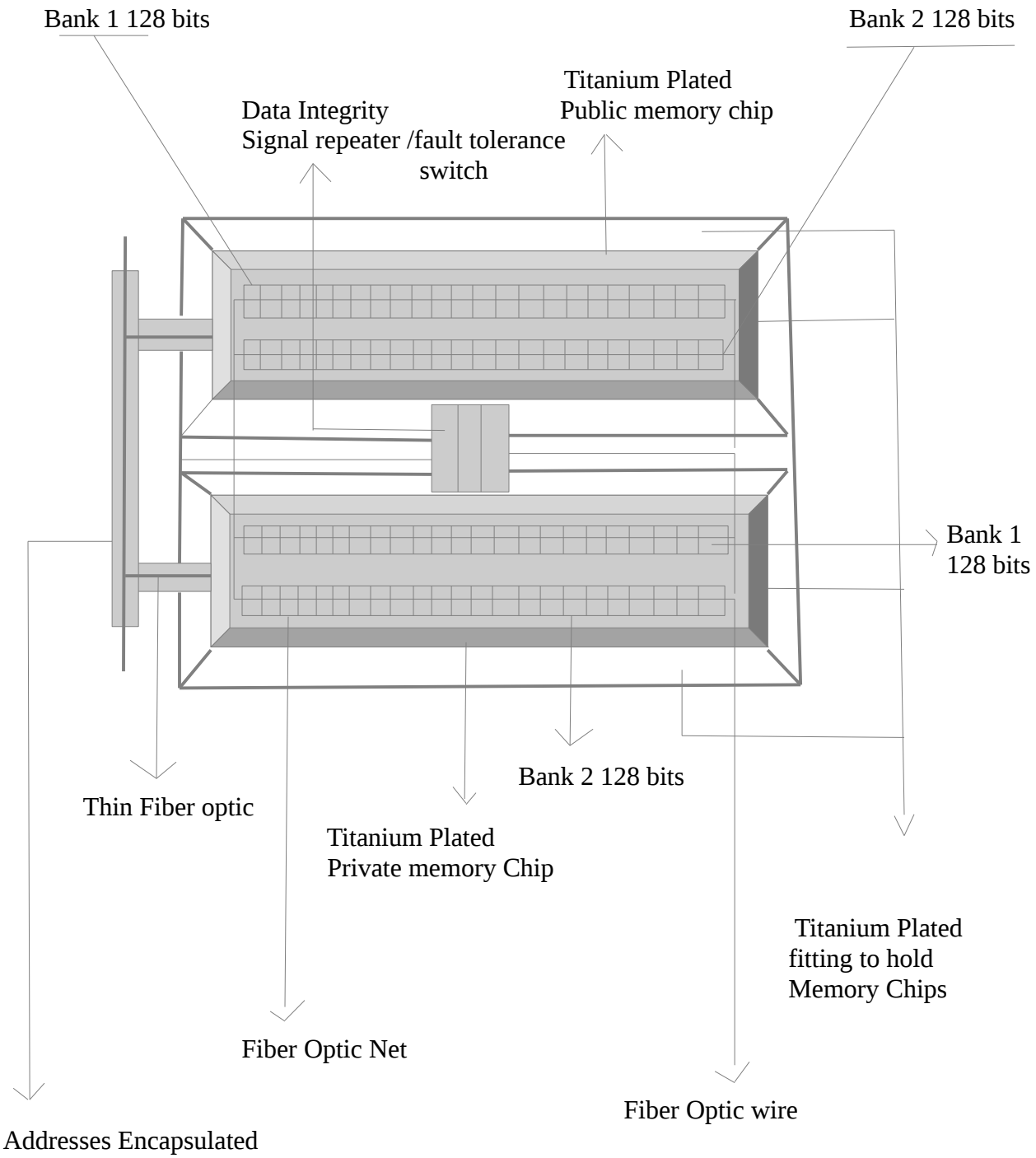


**Model Super Sonic 65 Motherboard- Design 4-B rev 1.2**

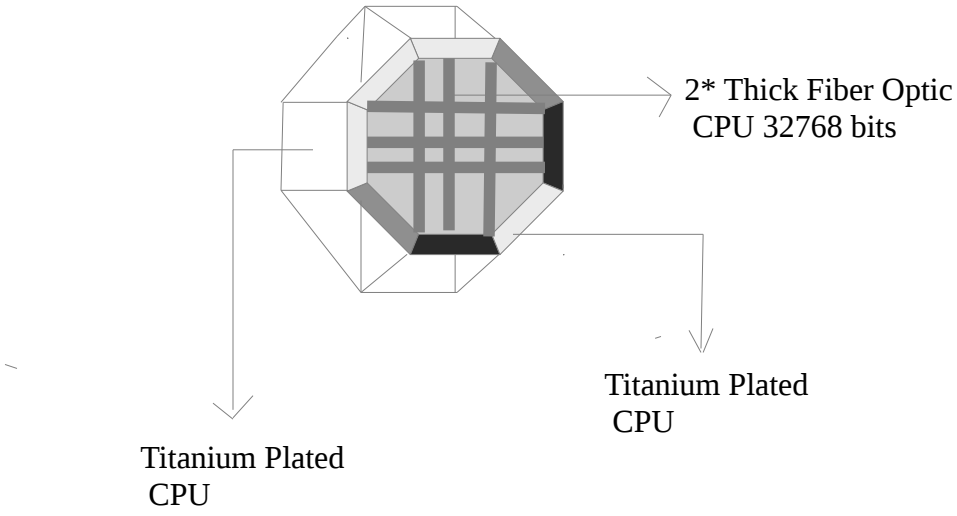


**Model Super Sonic 65 Motherboard- Design 5-B 1.2**

**128/256 Bit Instruction Set**



**Model Super Sonic 65 Motherboard- Design 6-B 1.2**



## Overview of Design

I would like to provide a brief overview of this design. I am taking a solar panel and using the energy to convert this to Mechanical. This is determined by a metric based system or a snapshot of how much energy is being utilized and it than routes this to the appropriate Area of Space which is in relations to the type of material that is being used. Example is I have just polled and took a snapshot of the energy and it is determined to be 4096 bits I than use the table and it is determined to use copper wire to transport the bits see chart 1-A and 2-A.

The second part is the Motherboard itself. As you can see the material being used has a higher heat tolerance than the standard motherboard do to the usage of Titanium on critical components such as the CPU and Memory Chips. Please note there is a limited amount of Optical lens for allowance of more Energy or bits to be processed this allows for better Privacy and Security methods such as Encryption and Authentication methods. Presently, the specs for my Motherboard and a Interface would allow for 19,456 bits the solar panel can push up to 32,768 bits as indicated in the table. The topography allows for a direct Interface rather than a shared resource such as a panel to Interface than to the Motherboard itself. The Visual Chart 6-B CPU uses a 2* Thick Fiber Optic to allow for **32,768 bits plated with Titanium**

I have updated the memory chip to process 128/256 bit Instruction Sets. The following specs maybe utilized. The 128 bit Instruction set allows for Fault tolerance by providing a check sum on addresses that utilize programs within memory-Data Integrity. If you wish not to use fault tolerance than the switch can be programmed for 256 bits no fault tolerance. Please also observe there are Public and Private memory chips labeled bank1 and bank 2. Please see specifications in next chapter 2-b and 3-b.

8 bits = 1 byte
2 bytes = 1 character

If we take 128 bits and divide it by 8 bits, I have 16 bytes. 16 bytes divide by 2 = 8 characters per field usually in traditional assembler you have 2 characters per field when you pack that leaves 1 character so this has expanded to 8 in a field packing leaves 4 characters so this produces instruction sets by a 4 to 1 ratio. I can expand the instruction set to allow for 256 bits if higher order Encryption, hashing and algorithms are desired with no fault tolerance but the default on the memory switch is set to 128 bits. Please also notice I have a Private and Public memory chips which means I have 2 input encoding and 4 outputs decoding – Private or Public.

The thin fiber optic that is attached to the memory chips provide protection of addresses thereby providing a level of security for programs that access the memory itself the idea of encapsulation bit at a address level. The addresses are encapsulated and services are only advertised on the board itself to protect against roaming wireless signals that advertise services that are undesired and unwanted.

In the next chapter, I will make a chart comparison of bits, bytes, and characters.

# Chapter 2

# Chart and Spec Comparisons

**Bit Strengths 2-B**

| # of bits | # of Bytes | # of characters/field |
|---|---|---|
| 8 | 1 | 1 |
| 16 | 2 | 1 |
| 32 | 4 | 2 |
| 64 | 8 | 4 |
| **128** | **16** | **8** |
| 256 | 32 | 16 |

Presently most operating software utilizes 64 bit operating systems Linux, Windows, etc. And after researching memory speeds reaching 1 billionths of a second commonly referred to as nano seconds the speeds of this design should be able to exceed present day speed levels roughly 2-4 times ;thereby, making time and space almost mote pointless. To support this idea please take 10 $-9^{th}$ power and multiply itself after doing this multiply 10 $-9^{th}$ power and multiply itself 3 times than 4 times.

This enforces the concept of partial binding of the mass of a object creating the concept of time and space formation at a new level micro nano quarks as stated in previous works the measurement should be micro nano seconds when measuring speeds that exceed nano seconds and memory chip speeds and providing the idea of time and space formation.

I would like to provide a Interesting idea where time is like a switch 1 = on 0 = off meaning if the time switch is set to 0 than time is off and is irrelevant this is proved by taking 10 $-9^{th}$ power .00000001 * .000000001 the calculation on my PC shows 0 some scientist say well you only have so many numbers allowed on a PC but to make a stronger argument I can take .00000001 * .00000001 * 00000001. The main idea is to show time becomes irrelevant on a sub nano scale thus the idea of time = space is not constant and is shown to be dynamic.

## Memory Specifications 3-B

| Banks | Public Memory | Private Memory | fault tolerance |
|---|---|---|---|
| 1 | 64 | | yes |
| 2 | 64 | | yes |
| 1 | 128 | | no |
| 2 | 128 | | no |
| 1 | | 64 | yes |
| 2 | | 64 | yes |
| 1 | | 128 | no |
| 2 | | 128 | no |

# Chapter 3

# Logic Gateways

In this chapter, I will process logic gateways specifically polling the Area of Spaces and taking snapshots and than interfacing with the motherboard itself. After the bits are processed the next step is to load the parameters of the instruction sets same process polling and taking snapshots with the system using a metric to determine whether to load fault tolerance or optimize memory instruction sets. A good example is CMOS where code is loaded but not seen another example is sub-atomic particles it is there but cannot be seen.

**Load Encryption-table-module-table**

| **Variable** | **Encryption strength # bits** |
|---|---|
| aCopperField | 2048 |
| bCopperfield | 4096 |
| c1xThinFiberopticfield | 8192 |
| d1xThickfiberopticfield | 16384 |
| e 2xThickfiberopticfield | 32768 |

The next step is to load the menu and Logic Gateways.

{

**Load Read-Only-memory-Table**

****************************************************************
****** ******
****** **Select " A-Copper Field"** ******
****** ******
****** **Select " B-Copper Field"** ******
****** ******
****** **Select " Thin Fiber Optic Field"** ******
****** ******
****** **Select " 1 X Thick Fiber Optic Field"** ******
****** ******
****** **Select " 2 X Thick Fiber Optic Field"** ******
****** ******
****************************************************************

**Rem This is a system level program that is not visible and is polled**
**Rem before running test conditions**

**Gateway-processing**

**Gateway-1 =f**
**Gateway-2 =g**
**poll f**
**poll g**

0 = “off”
1 = “on”
if f = “on”
goto Area-space-1
else
if g = “on”
goto Area-Space-2
else
if f and g = “off
poll f and G
exit

rem Area-spaces checking conditions on or off

**Area-space-1**
0 = “off”
1 = “on”
h = aCopperField
i = bCopperfield

rem set switches to on or off and check conditions
if h = “on”
set 2048-bits
move “2048” h
else
if i = “on”
set 4096-bits
move “4096” i
else
if h and i = “off”

goto **Gateway-processing**

**Area-Space-2**

0 = “off”
1 = “on”
x = c1xThinFiberopticfield
y = d1xThickfiberopticfield
z = e 2xThickfiberopticfiel

rem set switches to on or off and check conditions
if x = “on”
set 8192-bits
move “8192” x

else

if y = “on”
set 16384-bits
move “16384” i
else
if z = “on”
set 32768-bits
move “32768” x
else
if x, y, z = “off”

**goto Gateway-processing**
poll Read-Only-memory-table
rem proceed to Super sonic 65 motherboard
rem test memory switch check conditions load and define space

goto memory-module-table
exit }

**memory-module-table**

**Load memory-table-module-table**

| **Variable** | **Memory-specs # bits** |
|---|---|
| memory-switch-on-1 | |
| memory-space-fault-tolerance-1 | 128-bits |
| memory-switch-on-2 | |
| memory-space-optimize-2 | 256-bits |

**rem control is passed from gateway processing to**
*** memory-instruction-sets module loading table**
*** and testing switch on memory-chips**

0 = “off”
1 = “on”
if **Area-space-1** = “on”
j = memory-switch-on-1
k= memory-space-fault-tolerance-1
set j = “on”
set k= “on”
set 128-bits
move 128-bits k
else

```
 if Area-space-1 = “off”
Area-Space-2 = “on”
 l = memory-switch-on-2
m=  memory-space-optimize-2
set l  =  ”on”
set m = “on”
set 256-bits
move 256-bits m



clear table
 exit
```

This was a simple logic gate program to demonstrate the following

1). Solar Energy is used for the Solar Panel
2). Solar Panel than is converted to Mechanical Energy -Bits
3). The solar panel is than polled and a snapshot is taken
4). The Gateway processing logic control is than initiated as outlined above- **Gateway-processing**
5). **Gateway-processing** passes control to the **memory-module-table**
6). programs that reside in memory are accessed and loaded on the hard disk.

I will now present my final thoughts in the next chapter.

# Chapter 4

# Final Thoughts

## Final Thoughts

I have finished revising my Motherboard Design and demonstrating a concept of time and space that supports my past theories on time and space.

I have taken my Motherboard designed and provided enhancements by means of memory chips providing the following:

Fault Tolerances
Memory Optimization
Expanded instruction sets
Enhanced Data Security

Memory is measured in nano Seconds one billionths of a second or 10 $-9^{th}$ power by demonstrating a means of doubling all the way to Quadrupling hint 2-4 times measurements of time and space come to a point of being a non factor non existent. This was discussed in previous works dealing with Network Topology Designs $18^{th}$ and $20^{th}$ order.

The Big bang Theory supports Einsteins Theory of General Relativity but after completing this work and reflecting upon it I believe a new theory has emerged based on Intelligent Design called **Barrys Theory of Non-Relativity (**go ahead have a chuckle humor ) where time and space are not a factor when working on a Micro Nano scale this was shown mathematically by showing the following:

1). .000000001 10 -9th power
2). .000000001 10 -9th power * .000000001 10 -9th power
3). .000000001 10 -9th power * .000000001 10 -9th power * .000000001 10 -9th power
4). .000000001 10 -9th power * .000000001 10 -9th power * .000000001 10 -9th power * .000000001 10 -9th power

The bible wrote and made references to this in the book of Genesis by demonstrating a principle of When God created the heavens and the Earth it was void not being binded to time and space. This is demonstrated in application and principle by showing memory chips- time being set to 0 = off = partial binding which was demonstrated and supported by Network Topology 18th and 20th order.

This is a hard concept for Secular/Ivy league Scientist and Big bang supporters to accept and yes it is even mind boggling to comprehend this in principal and application but I think a new field that deserves attention is Quantum mechanics and micro sub scales this provides a way to balance Nature and Physical forces by demonstrating another idea of time formation begins at a micro sub-atomic scale which could be understood by the micro nano seconds in design and principle.

Intelligent Design has a place in Sciences because it has been shown Mathematically to be correct and is supported in this Science based work.

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